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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-1040

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/007,082 | MINNICK ET AL. | |
| | Examiner | Art Unit | |
| | Glenford Madamba | 2151 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Remarks*

1. This action is in response to remarks filed by Applicant's representative on May 29, 2007.

### *Response to Arguments*

2. With respect to Applicant's latest submission, the Office has given consideration to the remarks filed on October 18, 2007, but has deemed the arguments unpersuasive and/or insufficient to overcome the current rejection under Johnson and Duda provided in the previous Office Action, as will be discussed below.

With respect to claim 1, Applicant argues that the Johnson and Duda prior art references, either individually or in combination, does not teach nor disclose recited features of claim 1, which recites in part:

"moderate one or more interrupts to a processor if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency sensitive data."

The Office respectfully disagrees and submits that Applicant has misinerpreted and/or not fully considered all the teachings and disclosures of the Johnson and Duda prior art references.

In support of his argument, Applicant specifically argues that while Johnson discloses the I/O device (NIC) that is directed to improving data transfer latency, he does not teach '*using interrupts*' in any way to achieve this objective. Applicant also remarks that neither Johnson nor Duda teaches "moderating interrupts to a processor based on the characterization that received data fragments (packets) are *latency sensitive*. The Office respecftfully disagrees and asserts that Applicant has misinterpreted and/or not considered the full teachings and disclosures of the prior art references.

In response to the argument, the Office firstly remarks that Johnson expressly discloses the use and/or employment of *interrupts* (i.e., 'notifications' / 'interrupts' to the processors of data transfers and/or requests for data transfers) for embodiments that utilize a memory-mapped system or, alternatively, DMA systems. In particular, Johnson teaches that "for memory-mapped systems, the NIC informed the host processor, *usually by interrupt*, and the host processor controlled the transfer of the data from the buffer to the computer memory" [col 2, L.26-51]. With regards to DMA capable systems, Johnson teaches that "additional delays were necessary to configure a bus master device to perform the DMA transfer and to subsequently 'inform' the host

processor that the transfer was completed (e.g., by 'interrupt') [col 2, L55-59]. As disclosed by Johnson, 'advanced notification' to the host processor that data has been received from the network and is loaded into host memory is desirable and leads to overall reduction in latency when transferring data from a network to a computer system [col 3, L9-13] [col 4, L1-31] (e.g., 'the registers 310 enable passing of *interrupt signals* and status signals between the NIC 210 and the computer system 102") [col 6, L36-61]. The argued feature of 'moderating interrupts to a processor' is thus expressly disclosed by Johnson.

However, Johnson does not expressly disclose "moderating interrupts to a processor *based on the characterization that received data fragments are 'latency sensitive*". In Johnson, the packets received are 'generic' and all of packets received are handled in the same manner. In other words, Johnson discloses moderating interrupts for 'packets' in general, but does not disclose implementing the invention by identifying and/or distinguishing 'packets' received as 'latency sensitive' (having some time-criticality, priority, type, and/or size) as opposed to 'regular packets' received (non-latency sensitive packets). This deficiency of Johnson is resolved by Duda in a related endeavor.

Duda discloses as his invention a *Scheduling Algorithm* that fairly allocates a resource (e.g., CPU control / utilization) to a number of schedulable elements of which some are *latency-sensitive* (e.g., Video packets/frames) [col 1, L65-67]. The invention

enforces long-term fairness to each element while allowing latency-sensitive elements to be preferably selected (over non-latency sensitive elements / packets) [Abstract] [col 1, L65 – col 2, L467] [Figs. 1, 2a-b, 3]. For example, and with reference to Figures 2a-b and Figure 3, Duda expressly discloses "moderating interrupts to a processor *based on the characterization that received data fragments are 'latency sensitive*". Duda expressly discloses that Data Switch 200 examines the contents of the data packet and determines the service requirements and destination output port or ports required by the packet. The data packet is then queued into one of the queues that feed the specified output port, and 'queue selection' is based on the data packet's 'service requirements' (for example, latency sensitive data packets can be placed in a different queue than latency insensitive packets, or multicast packets).

Duda additionally discloses the implementation of a *Preemptive Scheduling Process* that is used to schedule a resource among a plurality of elements and is *"interrupt driven"*. Duda also teaches that the preemptive scheduling algorithm can be performed / implemented by a *computer* executing procedures, as well as by other 'mechanisms' (I/O devices), such as a *Data Switch 200*, which can also effectuate *Preemptive Scheduling Process 300* [col 5, L3 – col 6, L26]. In the computer context (initiated from within the processor), 'system timer interrupts' are initiated; in the data switch context, the preemptive scheduling process 300 is "interrupt driven" and employs *timer interrupts* as well as *enter timing interrupt, prior art interrupt, and return from interrupt* procedures to allow an element to have exclusive access to the resource from some number of

clock ticks [col, 6, L-27]. With reference to Figures 7, 10 and 11, Duda additionally teaches 'updating virtual time' that can be invoked when the 'condition' blocking the execution of a thread is satisfied (e.g., *device interrupt*, or some other condition or exception). Referencing Figure 10, Duda discloses *virtual time borrowing process 1000* that is prefatory to executing *latency-senstive code*. [col 12, L28-26]. The argued limitation of "moderating interrupts to a processor *based on the characterization that received data fragments are 'latency sensitive*" is thus expressly disclosed by Duda.

Given the above reasoning and justifications, it is clear from the teachings and disclosures of the prior art references that the combination of Johnson and Duda teaches all the required features of claim 1, as recited by the claim. Accoridngly, the rejection of claim 1 is maintained by the Office.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 22, 20 and 29 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson, U.S. Patent 5,905,874 in view of Duda et al (hereinafter Duda), U.S. Patent Number 7,065,762 B1.

As per claim 1, Johnson in view of Duda discloses an apparatus comprising:

an input/output (I/O) device **210** [Figs. 2 & 3] being operative to:

receive a fragment of electronic data [Col 2, Lines 27-42] from a node on a network;

determine the characteristics of the fragment of electronic data; [Duda: col 5, L2] and

moderate one or more interrupts to a processor [Duda: col 5, L57 –col 6, L17] [Fig. 3] if the characteristics of the fragment of electronc data indicate that the fragment of electronic data is latency-sensitive data [Duda: col 5, L3-23] [Fig. 2B].

While Johnson discloses substantial features of the invention such as I/O device to receive packets and/or portions of packets (fragments) and initiating interrupts, as above, he does not explicitly disclose the additional features of determining the characteristics of the fragment of electronic data; and moderating one or more interrupts to a processor if the characteristics of the fragment of electronc data indicate that the fragment of electronic data is latency-sensitive data. The features are expressly disclosed by Duda in a related endeavor.

Duda discloses as his invention a scheduling mechanism that fairly allocates a resource to a number of schedulable elements of which some are *latency-sensitive.* The invention enforces long-term fairness to each element while allowing *latency-sensitive* elements to be preferably selected [Abstract] [col 2, L43-60]. In particular, Duda expressly discloses the additional recited features of determining the characteristics of the fragment of electronic data (e.g., "latency-sensitivity characteristics) [col 5, L2]; and moderating one or more interrupts to a processor [col 5, L57 –col 6, L17] [Fig. 3] if the characteristics of the fragment of electronc data indicate that the fragment of electronic data is latency-sensitive data (e.g., "the packet dispatch mechanism *253 examines the contents of the data packet*, and determines the level service and output port(s) required by the data packet; determining if packet content is "*latency-sensitive or latency-insensitive*") [col 5, L3-23] [Fig. 2B].

It would thus be obvious to one of ordinary skill in the art at the time of the invention to combine and/or modify Johnson's invention with additional feature of determining the characteristics of the fragment of electronic data; and moderating one or more interrupts to a processor if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency-sensitive data, as disclosed by Duda, for the motivation of advantageously scheduling a resource between elements to maintain a fair long-term allocation of the resource to elements while still satisfying the responsive needs of latency-sensitive elements and to improve device performance [co 2, L29-40].

Claims 11, 20, and 29 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claim 3, Johnson dislcoses the apparatus of claim 1, wherein said I/O device comprises a network interface card (NIC) **210** [Col 2, lines 13-26; Col 3, lines 15-32; Figure 2 and 3].

As per claim 5, Johnson discloses the apparatus of claim 1, wherein said I/O device is configured to moderate by substantially immediately asserting said one or more interrupts of said associated computing platform processor [Col 2, lines 48-51 & Col 7, lines 52-56].

2. Claims 2, 4, 12, 13, 21, 22, 30, 31 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson in view of Duda and in further view of Drottar et al (hereinafter Drottar), Patent Number 6,333,929.

As per claim 2, 12, 21 and 31, Johnson in view of Duda and in further view of Drottar discloses the apparatus of claim 1, wherein the latency-sensitive data comprises an acknowledgement (ACK).

Johnson teaches in his invention that data is typically transferred across network segments in the form of packets or frames. Further, the data transferred and written into the buffer of an I/O device, such as a network interface device (NIC), *are written in blocks of data that are in the form of packets or portions of packets* (fragments) [Col 2, Lines 27-42]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose that the portion of said contents of said fragment of data specifically comprises an acknowledgement (ACK).

Drottar, in his invention for formatting and transmitting network packets over a distributed computer system, discloses a packet format that includes a transaction header **640** and a media access control (MAC) header **650** [Col 3, lines 6-9; also Col 11, lines 16-19; Figure 6]. As can be seen in the format for data packets with a MAC header, the header format includes a field for an ACK/NAK identification and processing [Col 13, lines 1-7; also see Col 10, lines 59-67].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to include the packet formatting features employed by Drottar's invention into the combined invention of Johnson and Duda for the motivation of improving packet switching speed and processing efficiency in the transmission of data [Col 16, lines 1-12].

Claims 12 and 21 state the same limitations as Claim 2 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claims 4, 13, and 22, Johnson in view of Drottar discloses the apparatus of claim 1, wherein the latency-sensitive data comprises one or more data packets that have a priority designation [Drottar, Col 2, lines 31-33; also Col 16, lines 1-12 & 25-39].

Johnson teaches in his invention that data is typically transferred across network segments in the form of packets or frames. Further, the data transferred and written into the buffer of an I/O device, such as a network interface device (NIC), *are written in blocks of data that are in the form of packets or portions of packets* (fragments) [Col 2, Lines 27-42]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose that the portion of said contents of said fragment of data specifically comprises an acknowledgement (ACK).

Drottar, in his invention for formatting and transmitting network packets over a distributed computer system, discloses a packet format that includes a transaction header **640** and a media access control (MAC) header **650** [Col 3, lines 6-9; also Col 11, lines 16-19; Figure 6]. Drottar expressly teaches that the packet headers (MAC Header_650) are comprising *a priority field*, a version field and an address field [Drottar, Col 2, lines 31-33; also Col 16, lines 1-12 & 25-39].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to include the packet formatting feature of a field designating prioritization of packets transmitted or received, as disclosed by Drottar, the combined invention of

Johnson and Duda for the motivation of improving packet switching speed and processing efficiency in the transmission of data [Col 16, lines 1-12].

Claims 13 and 22 state the same limitations as Claim 4 above, and are rejected for the same reasons as they differ only by their statutory category.

3. Claims 6-10, 15-19, 24-28 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson in view of Duda and in further view of Gentry Jr., Patent Number 6,434,651.

As per claim 6, Johnson in view of Duda and in further view of Gentry discloses the apparatus of claim 1, wherein said I/O device is configured to moderate by deferring said one or more interrupts of said associated computing platform processor so that a predetermined number of interrupts per unit of time is not exceeded.

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the

packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose that the network interface device is configured to moderate by deferring one or more interrupts of the host processor so that a predetermined number of interrupts per unit of time is not exceeded.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, after one interrupt is issued to and serviced by a host processor, another interrupt in not generated until a *predetermined period of time* has passed for a specified amount of network traffic has been sent to the host computer system. [Gentry Jr., Col 7, lines 37-47 & 51-56; also Col 8, lines 1-11 & 39-67]

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the interrupt suppression features in Gentry Jr.'s invention into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface.

As per claims 7, 16, 25 and 30, Johnson in view of Duda and in further view of Gentry discloses states the apparatus of claim 1, wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular number of fragments

of electronic data of a particular type are received by said I/O device [Gentry Jr., Col 7, lines 19-36, 47-56, & 63-67; Col 8, lines 1-11 and 39-67].

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose the apparatus wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular number of fragments of electronic data of a particular type are received by said I/O device.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the apparatus wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular number of fragments of electronic data of a particular type are received by said I/O device [Gentry Jr., Col 7, lines 29-36].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the apparatus wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular number of fragments of electronic data of a particular type are received by said I/O in Gentry Jr.'s invention into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

Claims 16, 25 and 30 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claim 8, 17, and 26, Johnson in view of Duda and in further view of Gentry discloses the apparatus of claim 1, wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular quantity of electronic data is received [Gentry Jr., Col 7, lines 47-56, & 63-67; Col 8, lines 1-11].

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses

analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose the apparatus wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular quantity of electronic data is received.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the apparatus wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular quantity of electronic data is received [Gentry Jr., Col 7, lines 47-56, & 63-67; Col 8, lines 1-11].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the apparatus wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular quantity of electronic data is received in Gentry Jr.'s invention into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

Claims 17 and 26 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claim 9, 18, and 27, Johnson in view of Duda and in further view of Gentry discloses the apparatus of claim 1, wherein said moderation of associated computing platform interrupt scheme is configurable through a user interface.

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose the apparatus wherein said moderation of associated computing platform interrupt scheme is configurable through a user interface. Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the apparatus wherein said moderation of associated computing

platform interrupt scheme is configurable through a user interface [Gentry Jr., Col 7, lines 51-56; Col 8, lines 3-11].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the apparatus wherein said moderation of associated computing platform interrupt scheme is configurable through a user interface in Gentry Jr.'s invention into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

Claims 18 and 27 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claim 10, 19, and 28, Johnson in view of Duda and in further view of Gentry discloses the apparatus of claim 1, and further comprising: said I/O device further being operative to measure a particular period of time after the receipt of a fragment of electronic data, and further being operative to moderate one or more interrupts of an associated computing platform after said particular period of time has elapsed.

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for

communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose the apparatus further comprising: said I/O device further being operative to measure a particular period of time after the receipt of a fragment of electronic data, and further being operative to moderate one or more interrupts of an associated computing platform after said particular period of time has elapsed.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the apparatus further comprising: said I/O device further being operative to measure a particular period of time after the receipt of a fragment of electronic data, and further being operative to moderate one or more interrupts of an associated computing platform after said particular period of time has elapsed [Gentry Jr., Col 7, lines 37-47 & 51-56; also Col 8, lines 39-67].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the apparatus further comprising: said I/O device further being operative to measure a particular period of time after the receipt of a

fragment of electronic data, and further being operative to moderate one or more interrupts of an associated computing platform after said particular period of time has elapsed, as in Gentry Jr.'s invention, into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

Claims 19 and 28 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claim 15, Johnson in view of Duda and in further view of Gentry discloses the method of claim 11, wherein said moderating comprises deferring said one or more interrupts of said associated computing platform processor if a predetermined number of interrupts per unit time is met or exceeded

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and

Duda does not expressly disclose the method wherein said moderating comprises deferring said one or more interrupts of said associated computing platform processor if a predetermined number of interrupts per unit time is met or exceeded.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the method wherein said moderating comprises deferring said one or more interrupts of said associated computing platform processor if a predetermined number of interrupts per unit time is met or exceeded [Gentry Jr., Col 7, lines 37-47 & 51-56; also Col 8, lines 39-67].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the method wherein said moderating comprises deferring said one or more interrupts of said associated computing platform processor if a predetermined number of interrupts per unit time is met or exceeded, as in Gentry Jr.'s invention, into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

As per claim 24, Johnson in view of Duda and in further view of Gentry discloses the article of claim 20, wherein said moderating comprises deferring said interrupting of said associated computing platform processor.

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose the article wherein said moderating comprises deferring said interrupting of said associated computing platform processor.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the article wherein said moderating comprises deferring said interrupting of said associated computing platform processor [Gentry Jr., Col 1, Lines 5-10; Figure 1; also Col 7, lines 10-18].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the article wherein said moderating comprises

deferring said interrupting of said associated computing platform processor, as in Gentry Jr.'s invention, into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

## *Conclusion*

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenford Madamba whose telephone number is 571-272-7989. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Valencia Wallace Martin can be reached on 571-272-3440. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Glenford Madamba
Examiner
Art Unit 2151